SIS3300 AMANDA 2
65/80/100 MHz
VME FADCs

User Manual

SIS GmbH
Harksheider Str. 102A
22399 Hamburg
Germany

Phone: ++49 (0) 40 60 87 305 0
Fax: ++49 (0) 40 60 87 305 20

email: info@struck.de
http://www.struck.de

Dedicated Amanda 2 Firmware Version: 2.00 as of 14.01.04

Revision Table:

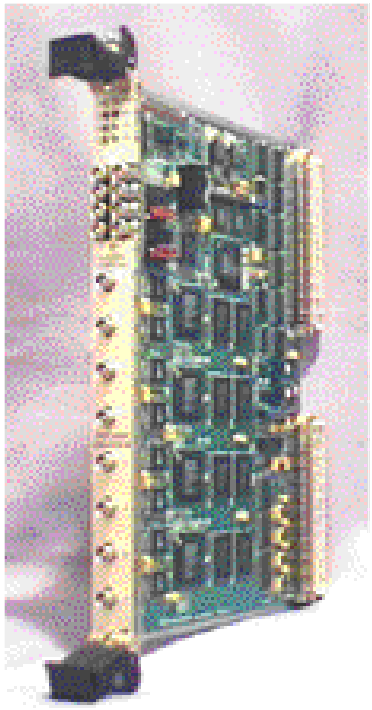
Revision	Date	Modification
2.00	14.01.04	Generated from general SIS330x V3.30

- Table of contents

1 Introduction

The SIS3300/3301 are eight channel ADC/digitizer boards with a sampling rate of up to 105 MHz (for the individual channel) and a resolution of 12/14-bit. The boards are single width 6U VME card, which has no special (i.e. non standard VME) voltage requirements.
Dual memory bank functionality in conjunction with multi event memory structure and a range of trigger options give the unit the flexibility to cover a variety of applications.

Applications comprise but are not limited to:
? digitization of “slow” detectors like calorimeters
? spectroscopy with Ge-detecors
? beam profile monitor readout
? serialized readout of ?-Strip detector data



This version of the documentation describes the firmware status that was developed for the Amanda Neutrino detector. The firmware was optimized for efficient sparsifying readout of multiple SIS3300 under control of the SIS9200 DSP option of the SIS3100 VME sequencer.
As we are aware, that no manual is perfect, we appreciate your feedback and will try to incorporate proposed changes and corrections as quickly as possible. The most recent version of this manual can be obtained by email from info@struck.de, the revision dates are online under http://www.struck.de/manuals.htm.

1.1 Related documents

A list of available firmware designs can be retrieved from
http://www.struck.de/sis3300firm.htm
The JTAG firmware installation procedure is described in
http://www.struck.de/sis3300_jtagprog.pdf

2 Technical Properties/Features

2.1 Key functionality

Find below a list of key features of the SIS3300 and SIS3301 digitizers.

	SIS3300	SIS3301-65	SIS3301-80	SIS3301-105
Sampling rate per channel	105 MHz	65 MHz	80 MHz	105 MHz
Minimum symmetric clock	1 MHz	15 MHz	15 MHz	15 MHz
Resolution	12-bit	14-bit	14-bit	14-bit
Analog bandwidth	> 80 MHz	35 MHz (1)	40 MHz	70 MHz
Typical pedestal variance	0.7 bit	1.1 bit (2)	1.1 bit (2)	1.1 bit (2)
Differential input version	-	X	X	X
2 x 128 KSample default	X	X	X	X
2 x 512 KSample option	-	X	X	X

(1) limited for better resolution
(2) with symmetric input range

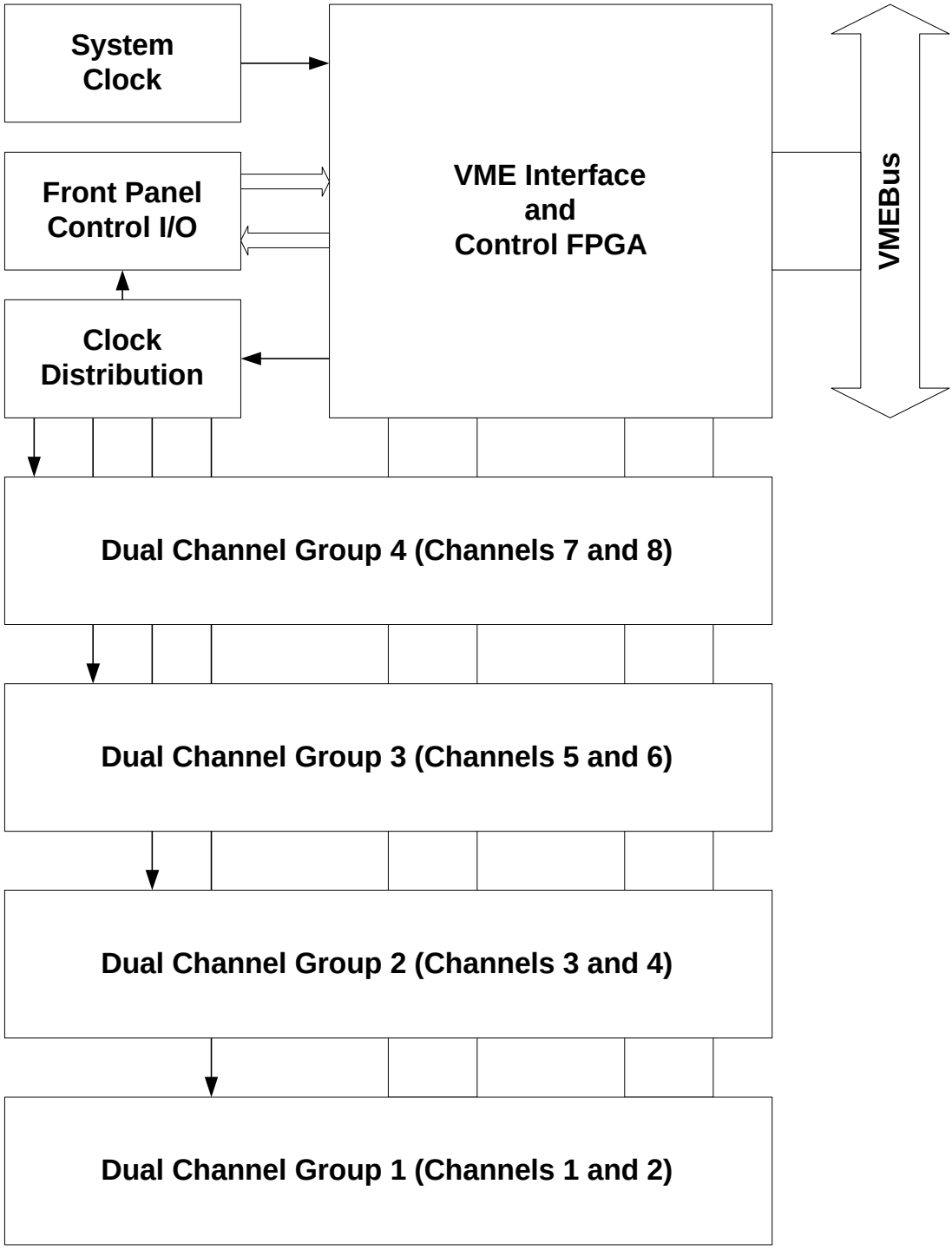
Common properties of all boards are:

? 8 channels
? special clock modes (clock prescaling, external “arbitrary” clock)
? channel to channel crosstalk below noise (i.e. invisible in Fourier spectrum)
? external/internal clock
? multi event mode
? Read on the fly (actual sample value)
? pre/post trigger option
? Two independent memory banks
? trigger generation
? 4 NIM control inputs/4 NIM control outputs
? A32 D32/BLT32/MBLT64/2eVME
? Geographical addressing mode (in conjunction with VME64x backplane)
? Hot swap (in conjunction with VME64x backplane)
? VME64x Connectors
? VME64x Front panel
? VME64x extractor handles (on request)
? F1002 compatible P2 row A/C assignment
? +5 V, +12V and –12 V VME standard voltages

Note: The SIS3300/1 shall not be operated on P2 row A/C extensions, like VSB e.g. due to the compatibility to the F1001 FADC modules clock and start/stop distribution scheme.

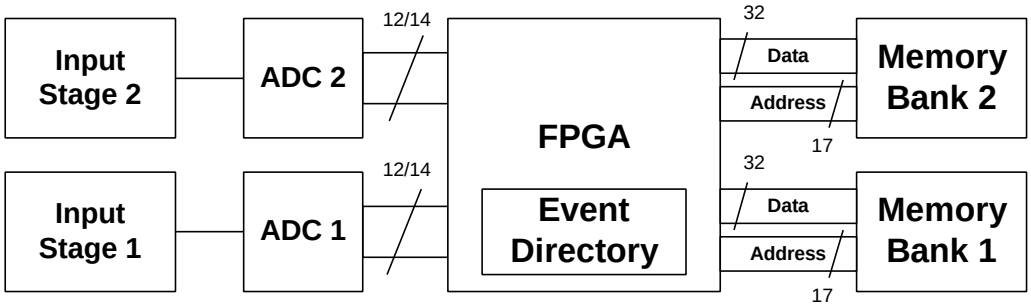
2.2 Module design

The SIS3300 consists of four identical groups of 2 ADC channels and a control section as shown in the simplified block diagram below.



2.2.1 Dual channel group

Two ADC channels form a group, which memory is handled by one Field Programmable Gate Array (FPGA).



2.3 Modes of Operation

The SIS3300 was developed with maximum flexibility in mind. The FPGA based design of the card allows to meet the requirements of many readout applications with dedicated firmware designs in the future. The initial firmware is supposed to furnish you with an easy to use yet powerful high speed high resolution Flash Analog to Digital Converter (FADC) implementation, that covers many everyday analog to digital applications.

2.4 Memory management

The individual memory bank(s) can be used either as one contiguous memory or as a subdivided multi event memory. In addition memory depth can be limited in single event operation to match the requirements of the given application. The memory configuration is defined through the memory configuration register, while bank handling (on dual memory bank modules) is under control of the acquisition control register.

2.5 Clock sources

The SIS3300/3301 features 3 basic clock modes

? Internal clock
? External symmetric clock

2.5.1 Internal clock

The internal clock is generated from an on board 40 or 50 MHz quartz. It is either doubled by a delay locked loop to 80/100 MHz or divided down to lower clock frequencies. The table below lists the valid clock settings for the different SIS3300/3301 boards.

Clock	SIS3300	SIS3301-65	SIS3301-80	SIS3301-105
100 MHz	X	-		X
80 MHz			X	
50 MHz	X	X		X
40 MHz			X	
25 MHz	X	X		X
20 MHz			X	
12.5 MHz	X	-		-
6.25 MHz	X	-		-
3.125 MHz	X	-		-

2.5.2 External clock

A symmetric external clock (NIM level, ratio between 45:55 and 55:45) can be fed to the module through a LEMO00 connector. An ECL clock over rows A/C of the J2 VME backplane can be used as an alternative. For optimum performance the clock frequency should be within the specified range for the given ADC chip.

Module	Min. sym. clock	Max sym. clock
SIS3300	1 MHz	105 MHz
SIS3301-65	15 MHz	65 MHz
SIS3301-80	15 MHz	80 MHz
SIS3301-105	15 MHz	105 MHz

2.6 VME Interrupts

Two registers, the Interrupt configuration and the Interrupt control register, are implemented for interrupt setup and control.
Three Interrupt sources are implemented:

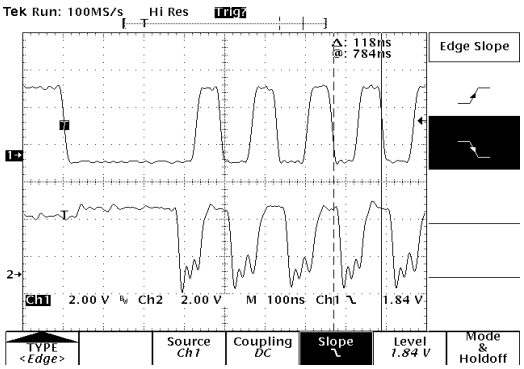
- External User Input (LEMO input 1)
- End Address Threshold valid (level sensitive)
- End Address Threshold valid (edge sensitive)

2.7 VME Readout Speed

The VME interface is optimized for readout speed. An internal FIFO/pipeline structure allows for high speed readout in block transfer mode (BLT32, MBLT64, 2eVME).
The timings below were measured with the SIS3100 (VME master) and the SIS3300/SIS3301 (VME Slave). The upper scope trace shows the VME signal DS1* (data strobe, low active). The VME Master asserts the DS1* to request (read) data.
The lower signal shows the VME signal DTACK* (Data Acknowledge, low active). The VME Slave asserts the DTACK* to acknowledge. that the data is valid on VME.

SIS330x DS* to DTACK* : 30-40ns

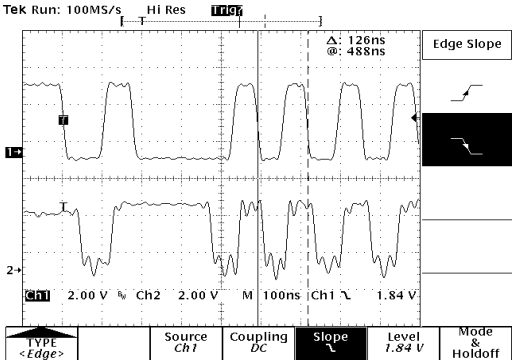
32bit every 120ns -- > **~ 33 MByte/sec**



BLT32

SIS330x DS* to DTACK* : 30-40ns

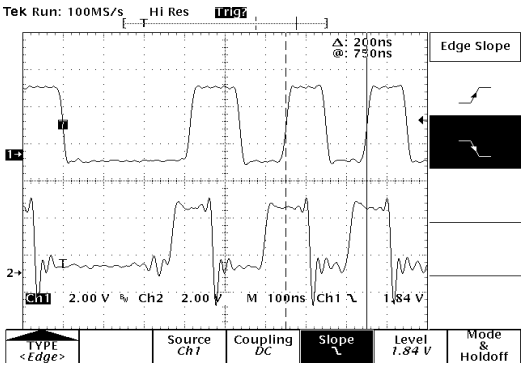
64bit every 125ns -- > **~ 64 MByte/sec**



MBLT64

SIS330x DS* to DTACK* : 50-60ns

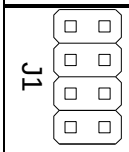
128bit every 200ns --> **~ 80 MByte/sec**



2eVME

3 VME Addressing

As the SIS3300 VME FADC features memory options with up to 2 banks of 4 times 128 K samples each, A32 addressing was implemented as the only option. Hence the module occupies an address space of 0xFFFFFF Bytes (i.e. 16 MBytes) are used by the module.
The SIS3300/1 firmware addressing concept is a pragmatic approach to combine standard rotary switch style settings with the use of VME64x backplane geographical addressing functionality.
The base address is defined by the selected addressing mode, which is defined by jumper array J1 and possibly SW1 and SW2 (in non geographical mode).

	Function
	EN_A32
	EN_GEO
	EN_VIPA
	reserved

The table below summarises the possible base address settings.

J1 Setting			Bits							
A32	GEO	VIPA	31	30	29	28	27	26	25	24
x			SW1				SW2			
x	x		0	0	0	GA4	GA3	GA2	GA1	GA0
		x	Not implemented in this design							

Shorthand	Explanation
SW1/SW2	Setting of rotary switch SW1 or SW2 respective
GA0-GA4	Geographical address bit as defined by the VME64x(P) backplane

Notes:

? This concept allows the use of the SIS3300/1 in standard VME as well as in VME64x environments, i.e. the user does not need to use a VME64x backplane.

? The factory default setting is EN_A32 closed, SW1=3, SW2=0 (i.e. the module will react to A32 addressing under address 0x30000000)

3.1 Address Map

The SIS3300 resources and their locations are listed in the table below.
Note: Write access to a key address (KA)with arbitrary data invokes the respective action

Offset	Size in Bytes	BLT	Access	Function
0x00000000	4	-	W/R	Control/Status Register (J-K register)
0x00000004	4	-	R	Module Id. and Firmware Revision register
0x00000008	4	-	R/W	Interrupt configuration register
0x0000000C	4	-	R/W	Interrupt control register
0x00000010	4	-	R/W	Acquisition control/status register (J-K register)
0x00000014	4	-	R/W	Broadcast setup register
0x00000020	4	-	KA W	General Reset
0x00000024	4	-	KA W	VME Clear 48-bit Timestamp Counter
0x00000030	4	-	KA W	VME Start sampling
0x00000034	4	-	KA W	VME Stop sampling
Event information all ADC groups				
0x00100000	4	-	W only	Trigger Configuration register (all ADCs)
0x00100020	4		W only	Trigger Threshold Detect register (all ADCs)
0x00100024	4		W only	Trigger Threshold End register (all ADCs)
0x00100028	4		W only	Trigger Threshold Overshot register (all ADCs)
0x0010002C	4		W only	End Address Threshold register (all ADCs)
Event information ADC group 1				
0x00200000	4	-	R/W	Trigger configuration register (ADC1, ADC2)
0x00200008	4	-	R	Bank1 address counter (ADC1, ADC2)
0x0020000C	4	-	R	Bank2 address counter (ADC1, ADC2)
0x00200018	4	-	R	Actual Sample Value (ADC1, ADC2)
0x0020001C	4	-	R	Actual Baseline Value (ADC1, ADC2)
0x00200020	4		R/W	Trigger Threshold Detect register (ADC1, ADC2)
0x00200024	4		R/W	Trigger Threshold End register (ADC1, ADC2)
0x00200028	4		R/W	Trigger Threshold Overshot register (ADC1, ADC2)
0x0020002C	4		R/W	End Address Threshold register (ADC1, ADC2)
Event information ADC group 2				
0x00280000	4	-	R/W	Trigger configuration register (ADC3, ADC4)
0x00280008	4	-	R	Bank1 address counter (ADC3, ADC4)
0x0028000C	4	-	R	Bank2 address counter (ADC3, ADC4)
0x00280018	4	-	R	Actual Sample Value (ADC3, ADC4)
0x0028001C	4	-	R	Actual Baseline Value (ADC3, ADC4)
0x00280020	4		R/W	Trigger Threshold Detect register (ADC3, ADC4)
0x00280024	4		R/W	Trigger Threshold End register (ADC3, ADC4)
0x00280028	4		R/W	Trigger Threshold Overshot register (ADC3, ADC4)
0x0028002C	4		R/W	End Address Threshold register (ADC3, ADC4)
Event information ADC group 3				
0x00300000	4	-	R/W	Trigger configuration register (ADC5, ADC6)
0x00300008	4	-	R	Bank1 address counter (ADC5, ADC6)
0x0030000C	4	-	R	Bank2 address counter (ADC5, ADC6)
0x00300018	4	-	R	Actual Sample Value (ADC5, ADC6)
0x0030001C	4	-	R	Actual Baseline Value (ADC5, ADC6)
0x00300020	4		R/W	Trigger Threshold Detect register (ADC5, ADC6)
0x00300024	4		R/W	Trigger Threshold End register (ADC5, ADC6)

0x00300028	4		R/W	Trigger Threshold Overshot register ADC5, ADC6)
0x0030002C	4		R/W	End Address Threshold register (ADC5, ADC6)
Event information ADC group 4				
0x00380000	4	-	R/W	Trigger configuration Register (ADC7, ADC8)
0x00380008	4	-	R	Bank1 address counter (ADC7, ADC8)
0x0038000C	4	-	R	Bank2 address counter (ADC7, ADC8)
0x00380018	4	-	R	Actual Sample Value (ADC7, ADC8)
0x0038001C	4	-	R	Actual Baseline Value (ADC7, ADC8)
0x00380020	4		R/W	Trigger Threshold Detect register (ADC7, ADC8)
0x00380024	4		R/W	Trigger Threshold End register (ADC7, ADC8)
0x00380028	4		R/W	Trigger Threshold Overshot (ADC7, ADC8)
0x0038002C	4		R/W	End Address Threshold register (ADC7, ADC8)
Bank 1 memory				
0x00400000	0x80000	BLT32/MBLT64/2eVME	R/W*	Bank 1 memory (ADC1, ADC2)
0x00480000	0x80000	BLT32/MBLT64/2eVME	R/W*	Bank 1 memory (ADC3, ADC4)
0x00500000	0x80000	BLT32/MBLT64/2eVME	R/W*	Bank 1 memory (ADC5, ADC6)
0x00580000	0x80000	BLT32/MBLT64/2eVME	R/W*	Bank 1 memory (ADC7, ADC8)
Bank 2 memory				
0x00600000	0x80000	BLT32/MBLT64/2eVME	R/W*	Bank 2 memory (ADC1, ADC2)
0x00680000	0x80000	BLT32/MBLT64/2eVME	R/W*	Bank 2 memory (ADC3, ADC4)
0x00700000	0x80000	BLT32/MBLT64/2eVME	R/W*	Bank 2 memory (ADC5, ADC6)
0x00780000	0x80000	BLT32/MBLT64/2eVME	R/W*	Bank 2 memory (ADC7, ADC8)

*W in D32 only (for memory test e.g.)

Note 1: The event information is identical for the four ADC groups (unless the module has a hardware problem), hence it will be sufficient for normal operation to retrieve the needed information from one group only.

Note 2: MBLT64 and 2eVME read access is supported from the memory banks only.

4 Register Description

The function of the individual registers is described in detail in this section.
The first line after the subsection header (in Courier font) like:

```
#define SIS3300_CONTROL_STATUS      0x0     /* read/write; D32 */
```

refers to the sis3300.h header file.

4.1 Control/Status Register(0x, write/read)

```
#define SIS3300_CONTROL_STATUS      0x0     /* read/write; D32 */
```

The control register is in charge of the control of basic properties of the SIS3300/1 board, like output signal assignment, in write access. It is implemented via a selective J/K register, a specific function is enabled by writing a 1 into the set/enable bit, the function is disabled by writing a 1 into the clear/disable bit (which location is 16-bit higher in the register). An undefined toggle status will result from setting both the enable and disable bits for a specific function at the same time. On read access the same register represents the status register.

Bit	write Function	read Function
31	Clear reserved 15 (*)	
30	Clear reserved 14 (*)	
29	Clear reserved 13 (*)	
28	Clear reserved 12 (*)	
27	Clear reserved 11 (*)	
26	Clear reserved 10 (*)	
25	Clear reserved 9 (*)	
24	Clear reserved 8 (*)	
23	Clear reserved 7 (*)	
22	Clear reserved 6 (*)	
21	Clear reserved 5 (*)	Status Start Input (LEMO IN 3)
20	Clear reserved 4 (*)	Status Stop Input (LEMO IN 2)
19	Clear reserved 3 (*)	Status P2_SAMPLE_IN
18	Clear reserved 2 (*)	Status P2_RESET_IN
17	Clear user output (*)	Status P2_TEST_IN
16	Switch off user LED (*)	Status User Input (LEMO IN 1)
15	Set reserved 15	Status Control 15
14	Set reserved 14	Status Control 14
13	Set reserved 13	Status Control 13
12	Set reserved 12	Status Control 12
11	Set reserved 11	Status Control 11
10	Set reserved 10	Status Control 10
9	Set reserved 9	Status Control 9
8	Set reserved 8	Status Control 8
7	Set reserved 7	Status Control 7
6	Set reserved 6	Status Control 6
5	Set reserved 5	Status Control 5
4	Set reserved 4	Status Control 4
3	Set reserved 3	Status Control 3
2	Set reserved 2	Status Control 2
1	Set user output (if bit 2 is not set)	Status User Output (1=output on, 0=output off)
0	Switch on user LED	Status User LED (1=LED on, 0=LED off)

(*) denotes power up default setting

4.2 Module Id. and Firmware Revision Register (0x4, read)

```
#define SIS3300_MODID              0x4       /* read only; D32 */
```

This register reflects the module identification of the SIS3300/1 and its minor and major firmware revision levels. The major revision level will be used to distinguish between substantial design differences and experiment specific designs, while the minor revision level will be used to mark user specific adaptations.

Bit	Function	Reading
31	Module Id. Bit 15	3
30	Module Id. Bit 14	
29	Module Id. Bit 13	
28	Module Id. Bit 12	
27	Module Id. Bit 11	3
26	Module Id. Bit 10	
25	Module Id. Bit 9	
24	Module Id. Bit 8	
23	Module Id. Bit 7	0
22	Module Id. Bit 6	
21	Module Id. Bit 5	
20	Module Id. Bit 4	
19	Module Id. Bit 3	0/1
18	Module Id. Bit 2	
17	Module Id. Bit 1	
16	Module Id. Bit 0	
15	Major Revision Bit 7	
14	Major Revision Bit 6	
13	Major Revision Bit 5	
12	Major Revision Bit 4	
11	Major Revision Bit 3	
10	Major Revision Bit 2	
9	Major Revision Bit 1	
8	Major Revision Bit 0	
7	Minor Revision Bit 7	
6	Minor Revision Bit 6	
5	Minor Revision Bit 5	
4	Minor Revision Bit 4	
3	Minor Revision Bit 3	
2	Minor Revision Bit 2	
1	Minor Revision Bit 1	
0	Minor Revision Bit 0	

4.2.1 Major revision numbers

Find below a table with major revision numbers used to date

Major revision number	Application/user
0x01 to 0x0F	Generic designs (03)
0x10	Amanda

4.3 Interrupt configuration register (0x8)

```
#define SIS3300_IRQ_CONFIG      0x8      /* read/write; D32 */
```

This read/write register controls the VME interrupt behaviour of the SIS3300 ADC. Four interrupt sources are foreseen, for the time being three of them are associated with an interrupt condition, the fourth condition is reserved for future use.
The interrupter type is DO8 .

4.3.1 IRQ mode

In RORA (release on register access) mode the interrupt will be pending until the IRQ source is cleared by specific access to the corresponding disable VME IRQ source bit. After the interrupt is serviced the source has to be activated with the enable VME IRQ source bit again.
In ROAK (release on acknowledge) mode , the interrupt condition will be cleared (and the IRQ source disabled) as soon as the interrupt is acknowledged by the CPU. After the interrupt is serviced the source has to be activated with the enable VME IRQ source bit again. ROAK IRQ mode can be used in conjunction with the University of Bonn LINUX Tundra Universe II driver by Dr. Jürgen Hannappel on Intel based VME SBCs.

Bit	Function	Default
31		0
...		0
16		0
15		0
14		0
13		0
12	RORA/ROAK Mode (0: RORA; 1: ROAK)	0
11	VME IRQ Enable (0=IRQ disabled, 1=IRQ enabled)	0
10	VME IRQ Level Bit 2	0
9	VME IRQ Level Bit 1	0
8	VME IRQ Level Bit 0	0
7	IRQ Vector Bit 7; placed on D7 during VME IRQ ACK cycle	0
6	IRQ Vector Bit 6; placed on D6 during VME IRQ ACK cycle	0
5	IRQ Vector Bit 5; placed on D5 during VME IRQ ACK cycle	0
4	IRQ Vector Bit 4; placed on D4 during VME IRQ ACK cycle	0
3	IRQ Vector Bit 3; placed on D3 during VME IRQ ACK cycle	0
2	IRQ Vector Bit 2; placed on D2 during VME IRQ ACK cycle	0
1	IRQ Vector Bit 1; placed on D1 during VME IRQ ACK cycle	0
0	IRQ Vector Bit 0; placed on D0 during VME IRQ ACK cycle	0

The power up default value reads 0x 00000000

4.4 Interrupt control register (0xC)

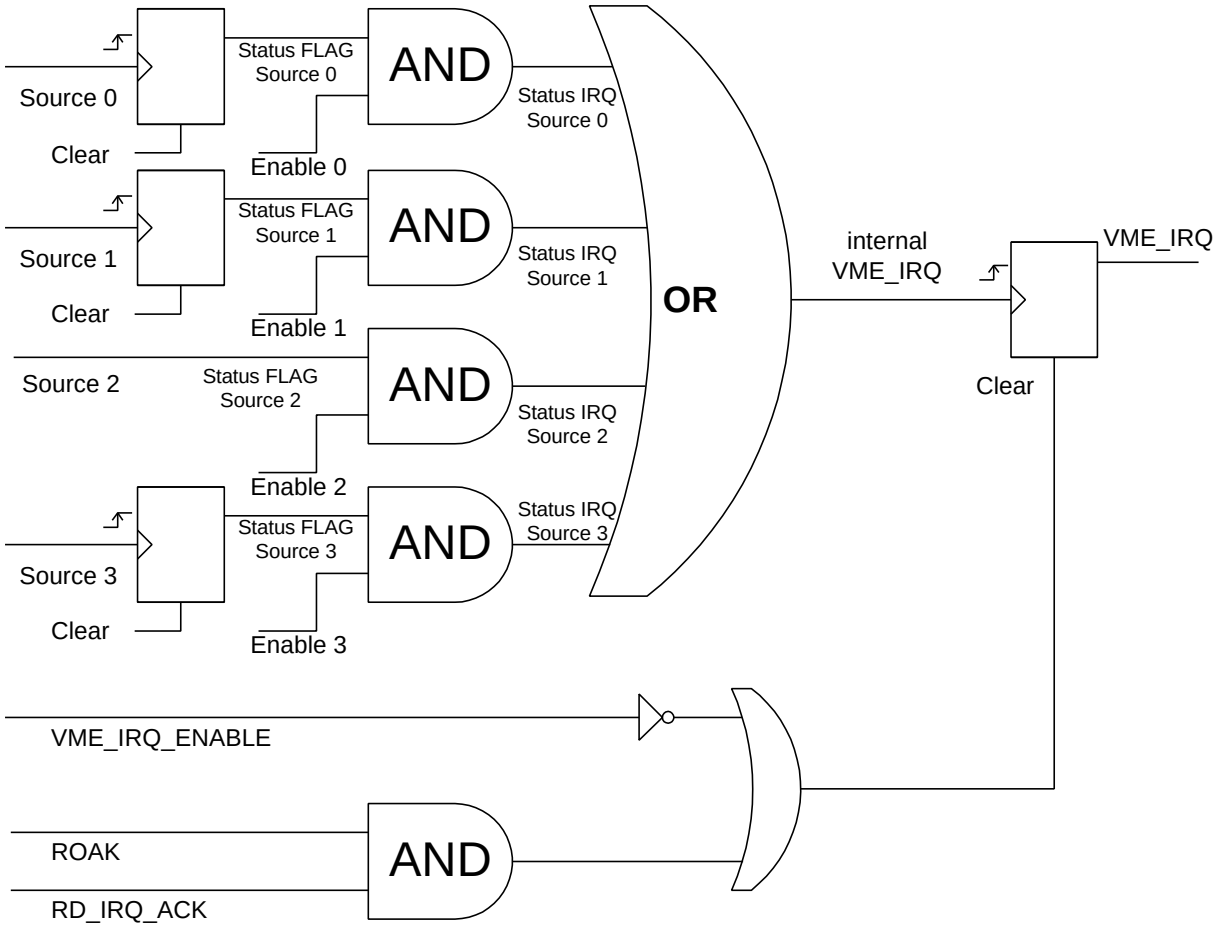
```
#define SIS3300_IRQ_CONTROL          0xC      /* read/write; D32 */
```

This register controls the VME interrupt behaviour of the SIS3300 ADC. Four interrupt sources are foreseen, for the time being three of them are associated with an interrupt condition, the fourth condition is reserved for future use.

Bit	Function (w)	(r)	Default
31	unused	Status IRQ source 3 (user input, edge sensitiv)	0
30	unused	Status IRQ source 2 (reserved)	0
29	unused	Status IRQ source 1 (End Address Threshold Flag; level sensitiv)	0
28	unused	Status IRQ source 0 (End Address Threshold Flag; edge sensitiv)	0
27	unused	Status VME IRQ	0
26	unused	Status internal IRQ	0
25	unused	0	0
24	unused	0	0
23	Clear IRQ source 3	Status flag source 3	0
22	Clear IRQ source 2	Status flag source 2	0
21	Clear IRQ source 1	Status flag source 1	0
20	Clear IRQ source 0	Status flag source 0	0
19	Disable IRQ source 3	0	0
18	Disable IRQ source 2	0	0
17	Disable IRQ source 1	0	0
16	Disable IRQ source 0	0	0
15	unused	0	0
14	unused	0	0
13	unused	0	0
12	unused	0	0
11	unused	0	0
...	...	...	0
4	unused	0	0
3	Enable IRQ source 3	Status enable source 3 (read as 1 if enabled, 0 if disabled)	0
2	Enable IRQ source 2	Status enable source 2 (read as 1 if enabled, 0 if disabled)	0
1	Enable IRQ source 1	Status enable source 1 (read as 1 if enabled, 0 if disabled)	0
0	Enable IRQ source 0	Status enable source 0 (read as 1 if enabled, 0 if disabled)	0

The power up default value reads 0x 00000000

The generation of the status flags, the IRQ flags and the actual IRQ is illustrated with the schematic below:



4.5 *Acquisition control register (0x10, read/write)*

```
#define SIS3300_ACQUISTION_CONTROL    0x10      /* read/write; D32 */
```

The acquisition control register is in charge of most of the settings related to the actual configuration of the digitization process.
Like the control register it is implemented in a J/K fashion.

Bit	Write Function	Read
31	Clear reserved	0
30	Clear Clock Source Bit2	0
29	Clear Clock Source Bit1	0
28	Clear Clock Source Bit0	0
27	Disable reserved	0
26	Disable front panel gate mode (not start/stop)	0
25	Disable P2 Start/Stop logic	0
24	Disable front panel LEMO start/stop logic	0
23	Disable P2 Clear Timestamp	0
22	Disable front panel Lemo Clear Timestamp	0
21	Disable reserved	0
20	Disable reserved	0
19	Disable reserved	0
18	Disable reserved	0
17	Disable sample clock for memory bank 2 (disarm sampling)	Status of End Address Threshold Flag
16	Disable sample clock for memory bank 1 (disarm sampling)	Status of ADC_BUSY (Gate)
15	Set reserved	0
14	Set clock source Bit 2	Status clock source Bit 2
13	Set clock source Bit 1	Status clock source Bit 1
12	Set clock source Bit 0	Status clock source Bit 0
11	Set reserved	Status reserved
10	Enable front panel gate mode (not Start/Stop)	Status front panel gate mode
9	Enable P2 Start/Stop logic	Status P2 start/stop logic
8	Enable front panel Lemo Start/Stop logic	Status front panel start/stop logic
7	Enable P2 Clear Timestamp (P2_RESET_IN)	Status P2 Clear Timestamp
6	Enable front panel Lemo Clear Timestamp (IN 1)	Status front panel Lemo Clear Timestamp
5	Enable reserved	Status reserved
4	Enable reserved	Status reserved
3	Enable reserved	Status reserved
2	Enable reserved	Status reserved
1	Enable Sample Clock for Memory Bank 2 (arm for sampling)	Status sample clock bank 2
0	Enable Sample Clock for Memory Bank 1 (arm for sampling)	Status sample clock bank 1

The power up default value reads 0x0

Clock source bit setting table:

Clock Source Bit2	Clock Source Bit1	Clock Source Bit0	Clock Source
0	0	0	internal 80/100 MHz
0	0	1	internal 40/50 MHz
0	1	0	internal 20/25 MHz
0	1	1	internal 12.5 MHz
1	0	0	internal 6.25 MHz
1	0	1	internal 3.125 MHz
1	1	0	external clock (front panel)
1	1	1	P2-Clock

Refer to the table in section 2.5.2for allowed clock speeds. Lower sampling rates into memory can be accomplished with random external clock mode.

4.6 Broadcast setup register

```
#define SIS3300A2_BROADCAST_SETUP        0x14  /* read/write; D32 */
```

This read/write register defines, whether the SIS3300 will participate in a Broadcast. The configuration of this register and the registers of other participating modules is essential for proper Broadcast behaviour.

Bit	Function
31	Broadcast address bit 31
30	Broadcast address bit 30
29	Broadcast address bit 29
28	Broadcast address bit 28
27	Broadcast address bit 27
26	Broadcast address bit 26
25	Broadcast address bit 25
24	Broadcast address bit 24
23	0
22	0
21	0
20	0
19	0
18	0
17	0
16	0
15	0
14	0
13	0
12	0
11	0
10	0
9	0
8	0
7	0
6	0
5	Enable Broadcast Master
4	Enable Broadcast
3	0
2	0
1	0
0	0

The power up default value reads 0x0

4.7 Key address general reset (0x20, write)

```
#define SIS3300_KEY_RESET                0x20  /* write only; D32 */
```

A write with arbitrary data to this register (key address) resets the SIS3300 to it's power up state.

4.8 Key address clear Timestamp (0x24, write)

```
#define SIS3300A2_KEY_CLEAR_TIMESTAMP    0x24  /* write only; D32 */
```

A write with arbitrary data to this register (key address) clears the 48-bit Timestamp Counter.

4.9 Key address VME start sampling (0x30, write)

```
#define SIS3300_KEY_START                0x30  /* write only; D32 */
```

A write with arbitrary data to this register (key address) will initiate sampling on the active memory bank if a bank is armed for sampling.

4.10 Key address VME stop sampling (0x34, write)

```
#define SIS3300_KEY_STOP                 0x34  /* write only; D32 */
```

A write with arbitrary data to this register (key address) will halt sampling on the active bank.

4.11 Trigger configuration registers (0x100000,0x200000,0x280000,0x300000,0x380000)

```
#define SIS3300A2_TRIGGER_CONFIG_ALL_ADC   0x100000   /* write only;D32 */

#define SIS3300A2_TRIGGER_CONFIG_ADC12     0x200000   /* read/write;D32 */
#define SIS3300A2_TRIGGER_CONFIG_ADC34     0x280000   /* read/write;D32 */
#define SIS3300A2_TRIGGER_CONFIG_ADC56     0x300000   /* read/write;D32 */
#define SIS3300A2_TRIGGER_CONFIG_ADC78     0x380000   /* read/write;D32 */
```

Bit	function
31	unused; read 0
19	unused; read 0
19	unused; read 0
20	N_FOLLOWING Bit 4
19	N_FOLLOWING Bit 3
23	N_FOLLOWING Bit 2
23	N_FOLLOWING Bit 1
20	N_FOLLOWING Bit 0
23	unused; read 0
22	unused; read 0
21	unused; read 0
20	N_PRECEEDING Bit 4
19	N_PRECEEDING Bit 3
18	N_PRECEEDING Bit 2
17	N_PRECEEDING Bit 1
16	N_PRECEEDING Bit 0
15	Programmable Header Bit 7
14	Programmable Header Bit 6
13	Programmable Header Bit 5
12	Programmable Header Bit 4
11	Programmable Header Bit 3
10	Programmable Header Bit 2
9	Channel Group ID Bit 1 (only read)
8	Channel Group ID Bit 0 (only read)
7	unused; read 0
6	unused; read 0
5	unused; read 0
4	unused; read 0
3	unused; read 0
2	unused; read 0
1	Baseline Average Bit 1
0	Baseline Average Bit 0

The power up default values of the registers are:

```
SIS3300A2_TRIGGER_CONFIG_ADC12:     0x00000000
SIS3300A2_TRIGGER_CONFIG_ADC34:     0x00000100
SIS3300A2_TRIGGER_CONFIG_ADC56:     0x00000200
SIS3300A2_TRIGGER_CONFIG_ADC78:     0x00000300
```

(i.e. the two channel group ID bits identify the four channel groups)

4.11.1 Baseline Average Bits

The Baseline Average Bits defines number of samples for the averaging of the "moving" Baseline:

Baseline Average Bit 1	Baseline Average Bit 0	Number of samples
0	0	16
0	1	32
1	0	64
1	1	128

Note: Issue a Baseline Reset (enable Bank1 or Bank2) after changing the Baseline Average bit setting

4.11.2 Programmable Header Bits

Six programmable header bits and two fix header bits are implemented to determine the ADC channel.

4.11.3 N_PRECEEDING Bits and N_FOLLOWING Bits

In order to get reasonable information about the pulse "begin and end", a defined number of presamples and postsamples are programmable.

The possible number of presamples (N_PRECEEDING) are between 0 and 24 (0x18).
If the number is higher than 24 (25 to 31) the number is set to 24.

The possible number of postsamples (N_FOLLOWING) are between 0 and 31.

4.12 Trigger Threshold Detect registers (0x100020, 0x200020, 0x280020, 0x300020, 0x380020)

```
#define SIS3300A2_THRESHOLD_DETECT_ALL_ADC  0x100020  /* write only;D32 */

#define SIS3300A2_THRESHOLD_DETECT_ADC12    0x200020  /* read/write;D32 */
#define SIS3300A2_THRESHOLD_DETECT_ADC34    0x280020  /* read/write;D32 */
#define SIS3300A2_THRESHOLD_DETECT_ADC56    0x300020  /* read/write;D32 */
#define SIS3300A2_THRESHOLD_DETECT_ADC78    0x380020  /* read/write;D32 */
```

These read/write registers hold the "trigger threshold detect" values for the ADC channels 1/3/5/7 and 2/4/6/8.

Bit	31-28	27-16	15-12	11-0
Function	unused	threshold DETECT value ADC 1/3/5/7	unused	threshold DETECT value ADC 2/4/6/7

The power up default value reads 0x0

4.13 Trigger Threshold End registers (0x100024, 0x200024, 0x280024, 0x300024, 0x380024)

```
#define SIS3300A2_THRESHOLD_END_ALL_ADC  0x100024  /* write only;D32 */

#define SIS3300A2_THRESHOLD_END_ADC12    0x200024  /* read/write;D32 */
#define SIS3300A2_THRESHOLD_END_ADC34    0x280024  /* read/write;D32 */
#define SIS3300A2_THRESHOLD_END_ADC56    0x300024  /* read/write;D32 */
#define SIS3300A2_THRESHOLD_END_ADC78    0x380024  /* read/write;D32 */
```

These read/write registers hold the "trigger threshold end" values for the ADC channels 1/3/5/7 and 2/4/6/8.

Bit	31-28	27-16	15-12	11-0
Function	unused	threshold END value ADC 1/3/5/7	unused	Threshold END value ADC 2/4/6/7

The power up default value reads 0x0

4.14 Trigger Threshold Overshot registers (0x100028, 0x200028, 0x280028, 0x300028, 0x380028)

```
#define SIS3300A2_THRESHOLD_OVERSHOT_ALL_ADC  0x100028 /* write only;D32 */

#define SIS3300A2_THRESHOLD_OVERSHOT_ADC12    0x200028 /* read/write;D32 */
#define SIS3300A2_THRESHOLD_OVERSHOT_ADC34    0x280028 /* read/write;D32 */
#define SIS3300A2_THRESHOLD_OVERSHOT_ADC56    0x300028 /* read/write;D32 */
#define SIS3300A2_THRESHOLD_OVERSHOT_ADC78    0x380028 /* read/write;D32 */
```

These read/write registers hold the "trigger threshold overshot" values for the ADC channels 1/3/5/7 and 2/4/6/8.

Bit	31-28	27-16	15-12	11-0
Function	unused	threshold OVERSHOT value ADC 1/3/5/7	unused	Threshold OVERSHOT value ADC 2/4/6/7

The power up default value reads 0x0

4.15 End Address Threshold registers (0x10002C, 0x20002C, 0x28002C, 0x30002C, 0x38002C)

```
#define SIS3300A2_END_ADDRESS_THRESHOLD_ALL_ADC  0x10002C /* wr only;D32 */

#define SIS3300A2_END_ADDRESS_THRESHOLD_ADC12    0x20002C /* rd/wr;D32 */
#define SIS3300A2_END_ADDRESS_THRESHOLD_ADC34    0x28002C /* rd/wr;D32 */
#define SIS3300A2_END_ADDRESS_THRESHOLD_ADC56    0x30002C /* rd/wr;D32 */
#define SIS3300A2_END_ADDRESS_THRESHOLD_ADC78    0x38002C /* rd/wr;D32 */
```

These read/write registers hold the "end address threshold" values for the ADC channel groups.

The value of the active (sample clock bank x is enabled) Bank Address Counter will be compared with the value of the End Address Threshold value.
The End Address Threshold Flag will be set valid if the value of the Bank x Address Counter is higher or equal than/as the value of the Bank Address Counter.

Bit	31-17	16 - 0
Function	unused	End Address Threshold

The power up default value reads 0x0

4.16 Bank 1 address counter (0x200008, 0x280008, 0x300008, 0x380008)

```
#define SIS3300_BANK1_ADDR_CNT_ADC12        0x200008   /* read only;D32 */
#define SIS3300_BANK1_ADDR_CNT_ADC34        0x280008   /* read only;D32 */
#define SIS3300_BANK1_ADDR_CNT_ADC56        0x300008   /* read only;D32 */
#define SIS3300_BANK1_ADDR_CNT_ADC78        0x380008   /* read only;D32 */
```

These read only registers hold the current bank 1 address counter for ADC group 1/2/3/4 and bank. The counter is 17 –bit wide. The counter will change while the ADC is sampling, after the ADC was stopped, the stop position can be. The address counter points to the next memory location that will be written to.

Bit	31-17	16-0
Function	unused, read back as 0	address counter

The address counter is not in a defined state after power up or Key Reset

4.17 Bank 2 address counter (0x20000C, 0x28000C, 0x30000C, 0x38000C)

```
#define SIS3300_BANK2_ADDR_CNT_ADC12        0x20000C   /* read only;D32 */
#define SIS3300_BANK2_ADDR_CNT_ADC34        0x28000C   /* read only;D32 */
#define SIS3300_BANK2_ADDR_CNT_ADC56        0x30000C   /* read only;D32 */
#define SIS3300_BANK2_ADDR_CNT_ADC78        0x38000C   /* read only;D32 */
```

Same as bank 1 address counters, but for bank 2 of ADC groups 1/2/3/4.

4.18 Actual Sample registers (0x200018, 0x280018, 0x300018, 0x380018)

```
#define SIS3300_ACTUAL_SAMPLE_VALUE_ADC12   0x200018   /* read only;D32 */
#define SIS3300_ACTUAL_SAMPLE_VALUE_ADC34   0x280018   /* read only;D32 */
#define SIS3300_ACTUAL_SAMPLE_VALUE_ADC56   0x300018   /* read only;D32 */
#define SIS3300_ACTUAL_SAMPLE_VALUE_ADC78   0x380018   /* read only;D32 */
```

Read “on the fly” of the actual converted ADC values.
The registers are updated with every ADC clock, unless a concurrent VME read access is pending.
The register contents is refreshed and can be read any time (i.e. they are updated independent of the unarmed, armed, sampling state) as long as a sampling clock is distributed on the ADC board (internal clock or active/clocking external clock)

For SIS3300:

ADC 1 / 3 / 5 / 7			ADC 2 / 4 / 6 / 8		
D31:29	D28	D27:16	D15:13	D12	D11:0
0 0 0	OR bit	12-bit data	0 0 0	OR bit	12-bit data

OR: Out of range, set with over or underflow.

4.19 Actual Baseline registers (0x20001C, 0x28001C, 0x30001C, 0x38001C)

```
#define SIS3300_ACTUAL_BASELINE_VALUE_ADC12  0x20001C  /* read only;D32 */
#define SIS3300_ACTUAL_BASELINE_VALUE_ADC34  0x28001C  /* read only;D32 */
#define SIS3300_ACTUAL_BASELINE_VALUE_ADC56  0x30001C  /* read only;D32 */
#define SIS3300_ACTUAL_BASELINE_VALUE_ADC78  0x38001C  /* read only;D32 */
```

Read “on the fly” of the actual Baseline values.
The registers are updated with every ADC clock, unless a concurrent VME read access is pending.
The register contents is refreshed and can be read any time (i.e. they are updated independent of the unarmed, armed, sampling state) as long as a sampling clock is distributed on the ADC board (internal clock or active/clocking external clock)

Note:

For SIS3300:

ADC 1 / 3 / 5 / 7		ADC 2 / 4 / 6 / 8	
D31:28	D27:16	D15:12	D11:0
0 0 0 0	12-bit average data	0 0 0 0	12-bit average data

Note: Issue a Baseline Reset (enable Bank1 or Bank2) after changing the Baseline Average bit setting

4.20 Bank 1 memory (0x400000 – 0x5ffffc)

```
#define SIS3300_MEMBASE_BANK1_ADC12             0x400000
#define SIS3300_MEMBASE_BANK1_ADC34             0x480000
#define SIS3300_MEMBASE_BANK1_ADC56             0x500000
#define SIS3300_MEMBASE_BANK1_ADC78             0x580000

/* write D32; read D32, BLT32, MBL64, 2eVME; size: 0x80000 */
```

Bank1 memory is divided into 4 channel groups of 128 KSamples. The 32-bit wide memory locations hold the data of 2 ADCs each. Readout can be done with D32, BLT32, MBLT64 or 2eVME, for memory tests D32 write cycles only are supported.

Notes:

? "FIFO" block transfer cycles (i.e. readout from a constant VME address in block transfer) are supported from every channel group (internal 17-bit address counter, A18 to A2)

? 2eVME cycles have to start on a 0x100 boundary (0x0, 0x100, 0x200 ...)

4.21 Bank 2 memory (0x600000 – 0x7ffffc)

```
#define SIS3300_MEMBASE_BANK2_ADC12             0x600000
#define SIS3300_MEMBASE_BANK2_ADC34             0x680000
#define SIS3300_MEMBASE_BANK2_ADC56             0x700000
#define SIS3300_MEMBASE_BANK2_ADC78             0x780000
```

Bank 2 memory is installed to allow for parallel readout from one memory bank, while the other memory bank is acquiring data. The second memory bank has the same structure as bank 1.

5 Description of Sampling

5.1 General

The advantage of this SIS3300 Firmware “AMANDA 2” is that every TWR (SIS3300) ADC channel is sampling continuously and independently of the other channels.
The general idea is

1. that the TWR can detect a PMT pulse by itself.
2. that every pulse including some preceeding (N_PRECEEDING) and following (N_FOLLOWING) values around the pulse is written to memory as a waveform fragment.
3. That every fragment includes a timestamp representing the time of the “THRESHOLD DETECT”.

5.2 TRIGGER

Each channel generates its own “moving baseline” by calculating a running mean (over 16, 32, 64 or 128 samples) of the input values.

Sampling algorithm:

a) The TWR samples the signal continuously.

b) The N_PRECEEDING values before and the actual sample followed by all following values below the programmable threshold “THRESHOLD_END” are written to the memory if a value below a programmable threshold “THRESHOLD_DETECT” is detected.

c) After the sampled values exceeds the “THRESHOLD_END” the logic starts adding N_FOLLOWING values to the fragment.

   c1) GOTO b) if there is an additional sampled value below “THRESHOLD_DETECT” .

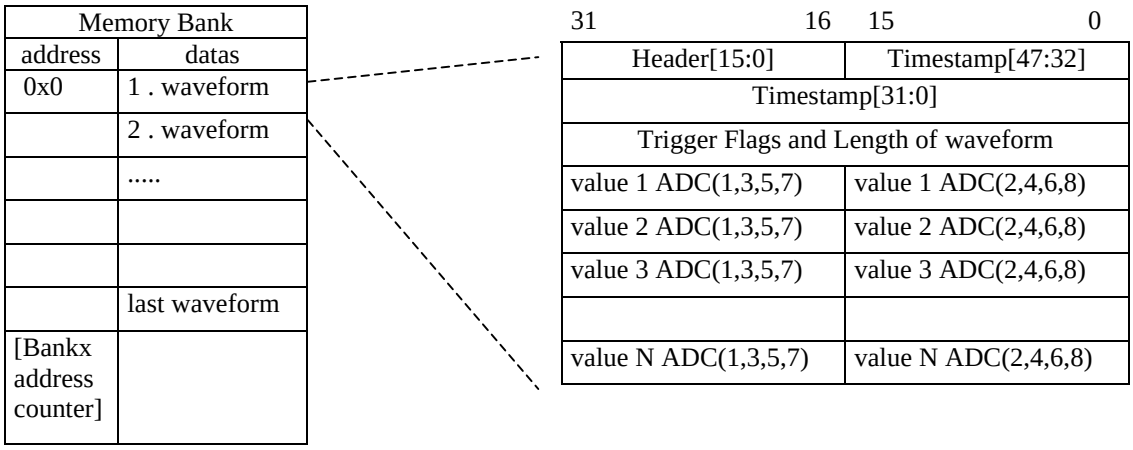
   c2) The N_FOLLOWING samples are just added if no further sampled values below “THRESHOLD_DETECT” .
   But if the sampled values are above “THRESHOLD_OVERSHOT” then the logic writes these values additional (to N_FOLLOWING) to the memory.

d) the fragment is closed

Note: Because two adc channels are assigned to one memoy bank the logic ors the Trigger Condition of the two channels. If one or both Trigger Condition(s) is/are true both ADC channels will be written to the memory.

5.3 Data Format

The sampled waveforms are written in the following data format to memory:



Header(16bit):

Header[15:8]	Header[7:2]	Header[1:0]
0x80	Programmable Header [7:2]	Channel Group ID Bit [1:0]

Trigger Flags and Length of waveform (32bit):

If the value of this register is 0xEEEEEEEE then the logic has aborted the sampling of this waveform
else

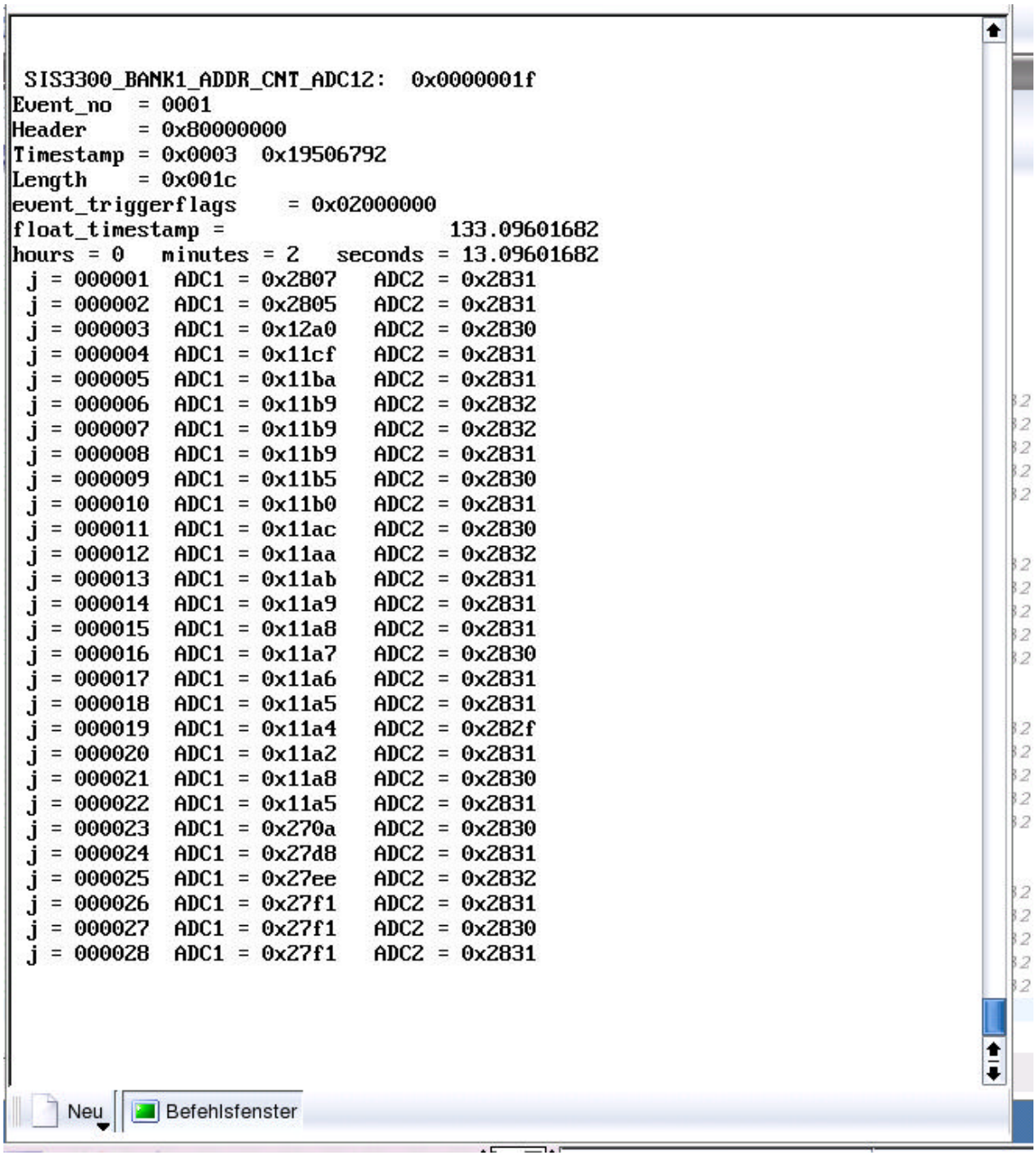
Bits [31:26]	Bit [25]	Bit [24]	Bits [23:17]	Bits [16:0]
0 0 0 0 0 0	ored DETECT_FLAG ADC(1,3,5,7)	ored DETECT_FLAG ADC(2,4,6,8)	0 0 0 0 0 0 0	Length of waveform

Value N (16bit):

Bit [15]	Bit[14]	Bit[13]	Bit[12]	Bits [11:0]
0	THRESHOLD OVERSHOT FLAG	THRESHOLD END FLAG	THRESHOLD DETECT FLAG	ADC Sample [11:0]

Example:

- 200 ns pulse on channel 1
- N_PRECEEDING = 2
- N_FOLLOWING = 6
- THRESHOLD DETECT = 0x400
- THRESHOLD END = 0x200



5.4 Operation

Configuration:

? Issue key reset

? define in Interrupt configuration register
- VME IRQ Level and Vector
- type of IRQ requester

? define in Broadcast Setup register
- define Broadcast VME address
- enable Broadcast Master
- enable Broadcast

? define in Interrupt control register
- enable IRQ source

? define in Acquistion register
- Set Clock source
- Set Start/Stop or Gate mode
- Enable/Disable P2 External Start/Stop
- Enable/Disable LEMO External Start/Stop
- Enable/Disable P2 External Clear Timestamp
- Enable/Disable LEMO External Clear Timestamp

? define in Trigger configuration register
- N_FOLLOWING
- N_PRECEEDING
- Programmable Header Bits
- Baseline Average Bits

? define in Trigger Threshold Detect registers
- THRESHOLD_DETECT for each channel

? define in Trigger Threshold End registers
- THRESHOLD_END for each channel

? define in Trigger Threshold Overshot registers
- THRESHOLD_OVERSHOT for each channel

? define in End Address Threshold registers
- memory bank threshold address for each channel group

5.4.1 Clear Timestamp:

- issue key Clear Timestamp or via external signal

5.4.2 sampling:

- Enable Sample Clock for Memory Bank1 (or Bank2)
- Issue key Start or External Start

- Poll on “End Address Threshold Flag” valid or IRQ

- Issue key Stop or External Stop
- Disable Sample Clock for Memory Bank1 (or Bank2)

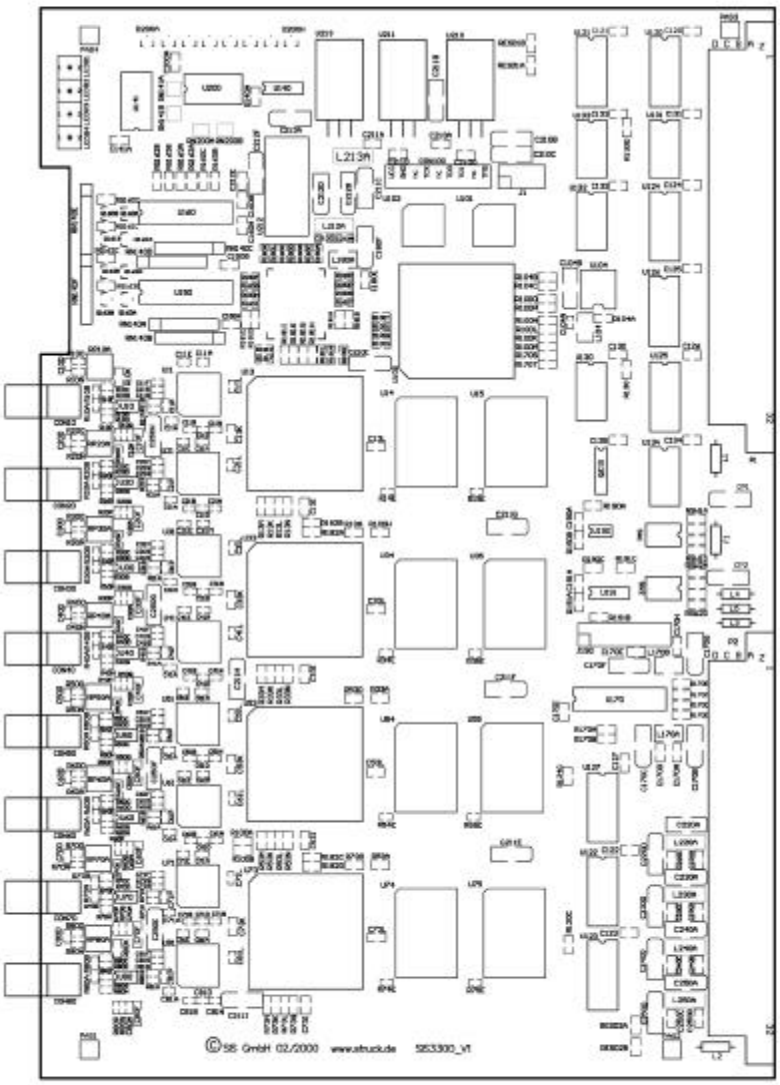
- Enable Bank2 and issue key Start and readout Bank1

5.4.3 readout:

- read Bank1 Address Counter for each ADC channel group (Bank1 is not enabled !)
- read Bank1 Memory for each ADC channel group until Bank1 Address Counter

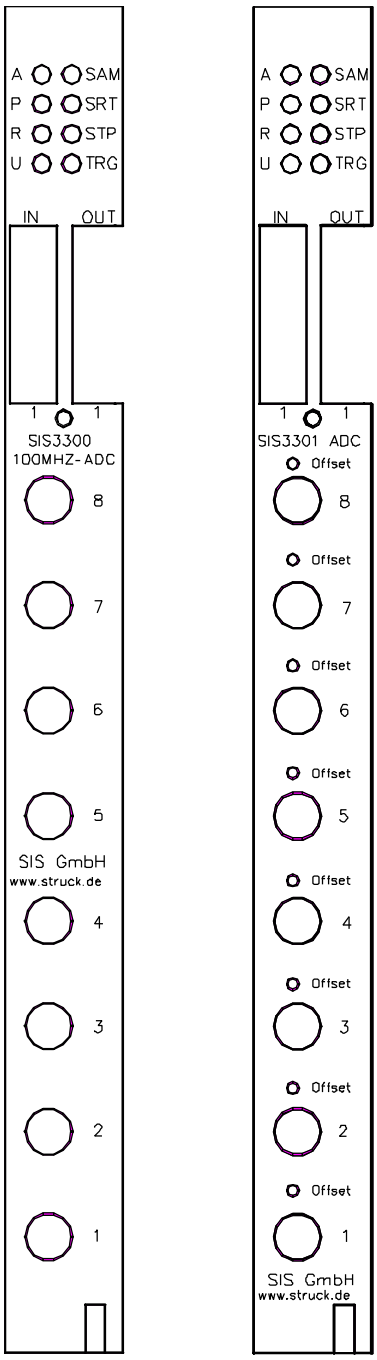
6 Board layout

A printout of the silk screen of the component side of the PCB is shown below.



7 Front panel

The SIS3300 is a single width (4TE) 6U VME module. A sketch of the SIS3300 (left hand side) and SIS3301 front panels (without handles) is shown below.



7.1 Control In/Outputs

The control I/O section features 8 LEMO00 connectors with NIM levels.

Designation	Inputs	Outputs	Designation
4	Clock In	Clock Out	4
3	Start	End Address Threshold	3
2	Stop	Trigger (write waveform to memory)	2
1	User in	User out	1

The external clock must be a symmetric signal unless the module is operated in external random clock mode
The width of an external start/stop pulse must be greater or equal two sampling clock periods.

7.1.1 User input

The User input could be used as Clear Timestamp Counter.

7.1.2 Control input termination

The control inputs are configured for 50 ? termination (i.e. with 47 ?) by default.
Each input is terminated with a resistor network (5 pins, 4 resistors, common pin to socket pin 6) to ground, the names of the input sockets are listed in the table below.

Designation	Inputs	Resistor Network
4	Clock In	RN140A
3	Start	RN140B
2	Stop	RN140C
1	User in	RN140D

7.2 Analog inputs

7.2.1 Input range and impedance configuration for single ended SIS3300/1

Input impedance and range are configured with a set of SMD resistors. The input range configuration is a combination of selecting the requried input voltage span and a possible input shift by means of a potentiometer. A unit with an input range of +2.5 V ... –2.5 V and a module with 0 V ... –5 V both have a span of 5 V, which is shifted by -2.5 V to the negative side in the later case e.g.

The table below lists the configuration for ADC channel 1. The other channels are configured with their corresponding resistors (R20A, ..., R20I for channel 7 e.g.).

Voltage span	Impedance	R10A	R10B	R10D	R10E	R10F	R10G	R10H	R10I
1 V	50 Ohm	50	0	560	1.2k	25	0	560	1.2k
2 V	50 Ohm	50	0	560	560	25	0	560	560
2 V	1 Kohm	1.2K	0	1.2k	1.2k	25	0	1.2k	1.2k
3 V	50 Ohm	50	680	33	511	25	680	33	511
4 V	50 Ohm	50	1k	15	560	25	1k	15	560
5 V	50 Ohm	50	1.2k	15	560	25	1.2k	15	560
8 V	75 Ohm	75	2k	0	560	33	2k	0	560

Note: defects that are due to in field input range configuration change are not covered by the modules warranty

7.2.2 Input range and impedance for differential SIS3301

The differential version of the SIS3301 has an input impedance of 100 Ohms and an input range of +1 V ... –1V.

7.3 LED's

The SIS3300 has 8 front panel LEDs to visualise part of the modules status. The user (and access) LED are a good way to check first time communication/addressing with the module.

Color	Designator	Function
Red	A	Access to SIS3300 VME slave port
Yellow	P	Power
Green	R	Ready, on board logic configured
Green	U	User, to be set/cleared under program control
Red	SAM	Lit if one Bank is enabled
Yellow	SRT	Lit if channels are sampling
Green	STP	Lit if End Address Threshold Flag is valid
Green	TRG	Trigger, lit if one or more channels are writing Waveforms to memory

The on duration of the access, sampling, start, stop and trigger LEDs is stretched to guarantee visibility even under low rate conditions.

7.4 PCB LEDs

The 8 surface mounted red LEDs D200A to D200H on the top left corner of the component side of the SIS3300 are routed to the control FPGA, their use may depend on the firmware design.

8 Jumpers/Configuration

8.1 J1

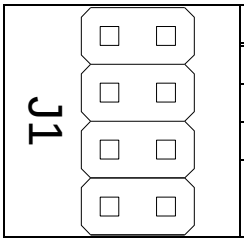
The function of J1 depends on the PCB (printed circuit board) revision level. The board revision level is printed in white on the lower edge of the card on the component side as a text of the form SIS3300_V1 e.g.

8.1.1 SIS3300_V1

Selection of bits 31-28 of the 32-bit A32 address (see. base address section)

8.1.2 SIS3300_V2 (and higher)

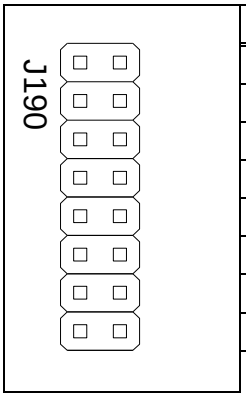
The SIS3300 supports several addressing modes, the actual mode is selected by jumper array J1. The given mode is selected if its corresponding jumper is in place. The four jumper positions are described in the table below. The A32 jumper is closest to the modules front panel.



Jumper	Function	Factory default
A32	enable A32 addressing	closed
GEO	enable geographical addressing	open
VIPA	not implemented yet	open
reserved	reserved	open

8.2 J190 Reset

Jumper 5 of jumper array J190 defines the reset behaviour of the SIS3300 upon VME Sysreset. If the jumper is closed the module will be reset with VME Sysreset. The other fields of the array are unused in the current firmware design.



Jumper	Function	Factory default
1	unused	open
2	enable watchdog	closed
3	unused	open
4	unused	open
5	unused	open
6	Connect module reset to VME_Sysreset	closed
7	unused	open
8	unused	open

The enable watchdog jumper has to be removed during the initial JTAG firmware load.

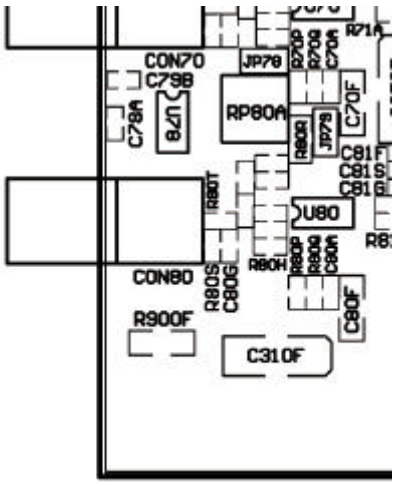
8.3 Offset adjustment

8.3.1 SIS3300

The pedestal or offset of single ended (non symmetric) ADC channels can be adjusted with the potentiometers RP10A through RP80A (see table below). The sensitivity for the positive or negative offset can be reduced by two limit jumpers (2 mm), the full range is available with both jumpers open. Do not install both jumpers for a channel in parallel.

channel	limit pos. offset	limit neg. offset	Offset-Potentiometer
1	JP78	JP79	RP80A
2	JP76	JP77	RP70A
3	JP58	JP59	RP60A
4	JP56	JP57	RP50A
5	JP38	JP39	RP40A
6	JP36	JP37	RP30A
7	JP18	JP19	RP20A
8	JP16	JP17	RP10A

The position of the two jumpers JP78 and JP79 close to potentiometer RP80A for ADC channel 1 is illustrated in the portion of the board shown below. The displayed area is the vicinity of the channel 1 LEMO input connector (CON80).



8.4 JTAG

The SIS3300 on board logic can load its firmware either from two serial PROMs or via the JTAG port on connector CON100. A list of firmware designs can be found under http://www.struck.de/sis3300firm.htm.
Hardware like the XILINX HW-JTAG-PC in connection with the appropriate software will be required for in field JTAG firmware upgrades.
The JTAG connector is a 9 pin single row 1/10 inch header, the pin assignment on the connector can be found in the table below.

Pin	Short hand	Description
1	VCC	Supply voltage
2	GND	Ground
3	nc	not connected, cut to avoid polarity mismatch
4	TCK	test clock
5	nc	not connected
6	TDO	test data out
7	TDI	test data in
8	nc	not connected
9	TMS	test modus

8.5 Power consumption

The SIS3300/1 is a single supply design to facilitate operation in any VME environment, i.e. the module does not require special backplanes or non standard VME voltages.
The power consumption of a two memory bank module digitizing at 100 MHz was measured to be:

Voltage	Current
+ 5V	< 6A
+12 V	< 40 mA
- 12 V	< 60 mA
P < 32 W	

8.6 Operating conditions

8.6.1 Cooling

Although the SIS3300/1 is mainly a 2.5 and 3.3 V low power design, substantial power is consumed by the Analog to Digital converter chips and linear regulators. Hence forced air flow is required for the operation of the board. The board may be operated in a non condensing environment at an ambient temperature between 10? and 40? Celsius. A power up warm up time of some 10 minutes is recommended to ensure equilibrium on board temperature conditions.

8.6.2 Hot swap/live insertion

Please note, that the VME standard does not support hot swap by default. The SIS3300 is configured for hot swap in conjunction with a VME64x backplane. In non VME64x backplane environments the crate has to be powered down for module insertion and removal.

8.7 Connector types

The VME connectors and the two different types of front panel connectors used on the SIS3300 are:

Connector	Purpose	Part Number
160 pin zabcd	VME P1/P2	Harting 02 01 160 2101
LEMO PCB	Coax. control connector	LEMO EPB.00.250.NTN
90^o PCB LEMO	Analog input connector	LEMO EPL.00.250.NTN
90^o PCB LEMO	Analog input connector (3301 differential input version)	LEMO EPG.00.302.NLN

8.8 P2 row A/C pin assignments

The P2 connector of the SIS3300 has several connections on rows A and C for the F1002 compatible use at the DESY H1 FNC subdetector. This implies, that the module can not be operated in a VME slot with a special A/C backplane, like VSB e.g.. The pin assignments of P2 rows A/C of the SIS3300 is shown below:

P2A	Function	P2C	Function
1	-5.2 V	1	-5.2 V
2	-5.2 V	2	-5.2 V
3	-5.2 V	3	-5.2 V
4	not connected	4	not connected
5	not connected	5	not connected
6	DGND	6	DGND
7	P2_CLOCK_H	7	P2_CLOCK_L
8	DGND	8	DGND
9	P2_START_H	9	P2_START_L
10	P2_STOP_H	10	P2_STOP_L
11	P2_TEST_H	11	P2_TEST_L
12	DGND	12	DGND
13	DGND	13	DGND
14	DGND	14	DGND
15	DGND	15	DGND
16	not connected	16	not connected
...	...	17	...
31	not connected	18	not connected

8.9 Row d and z Pin Assignments

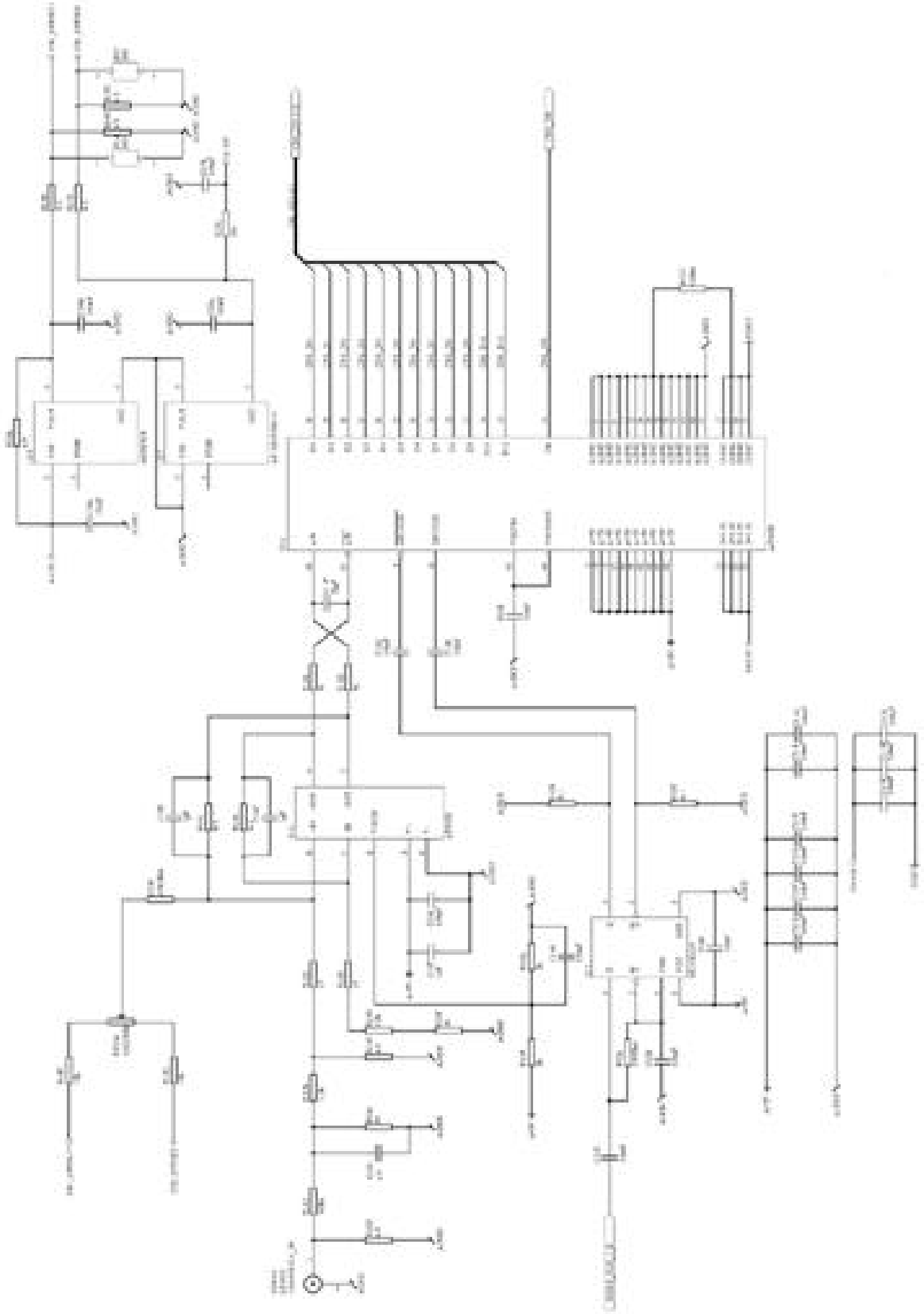
The SIS3300 is prepared for the use with VME64x and VME64xP backplanes. Foreseen features include geographical addressing (PCB revisions V2 and higher) and live insertion (hot swap). The prepared pins on the d and z rows of the P1 and P2 connectors are listed below.

Position	P1/J1		P2/J2	
	Row z	Row d	Row z	Row d
1		VPC (1)		
2	GND	GND (1)	GND	
3				
4	GND		GND	
5				
6	GND		GND	
7				
8	GND		GND	
9		GAP*		
10	GND	GA0*	GND	
11	RESP*	GA1*		
12	GND		GND	
13		GA2*		
14	GND		GND	
15		GA3*		
16	GND		GND	
17		GA4*		
18	GND		GND	
19				
20	GND		GND	
21				
22	GND		GND	
23				
24	GND		GND	
25				
26	GND		GND	
27				
28	GND		GND	
29				
30	GND		GND	
31		GND (1)		GND (1)
32	GND	VPC (1)	GND	VPC (1)

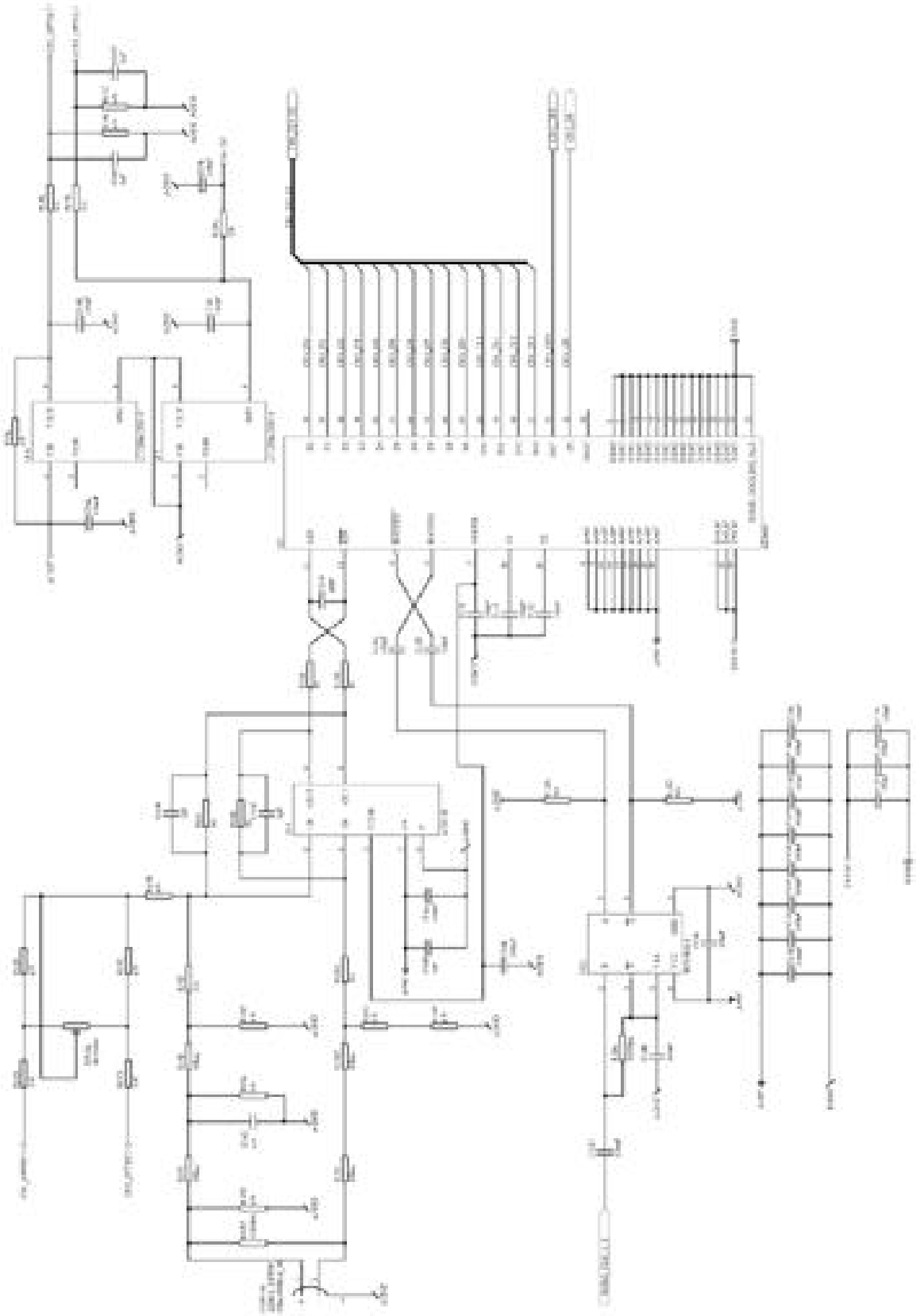
Note: Pins designated with (1) are so called MFBL (mate first-break last) pins on the installed 160 pin connectors, VPC(1) pins are connected via inductors.

8.10 Input Schematics

8.10.1 SIS330x (single ended)



8.10.2 SIS3301 (differential)



9 Index